



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

11/01

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,820	09/02/2003	Meng-Hsien Liu	406000	4148
27717	7590	08/24/2004	EXAMINER	
SEYFARTH SHAW 55 EAST MONROE STREET SUITE 4200 CHICAGO, IL 60603-5803			NGUYEN, JIMMY	
		ART UNIT	PAPER NUMBER	
			2829	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

HJD

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/653,820	LIU, MENG-HSIEN	
	<b>Examiner</b>	<b>Art Unit</b>	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 02 September 2003.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-7 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-7 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 02 September 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                     | Paper No(s)/Mail Date. _____ .  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____ .                                  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsai et al (US 5570375).

**As to claim 1**, Tsai et al disclose (fig 1) a circuit board having a boundary scan self-testing function, comprising:

a substrate (fig 1, a substrate in fig 1);

a plurality of devices under test (VLSI chip connects in series, fig 1) mounted on the substrate and having boundary scan circuits, and

an active testing device (20, 30 or 40, figs 6, 7, 8) mounted on the substrate (substrate in fig 1) and used for generating boundary scan testing data sequentially forwarding to the devices under test along a testing route.

**As to claims 2, 3, 7**, Tsai et al disclose (fig 1) a circuit board having a boundary scan self-testing function of claim 1, wherein the devices under test include programmable devices (VLSI chip, column 1 line 17 – 19).

**As to claim 4,** Tsai et al disclose (fig 1) a circuit board having a boundary scan self-testing function of claim 1, wherein the active testing device includes TCK, TMS and TRST pins which connect the devices under test in parallel, and further includes TDI and TDO pins which connect the devices under test in series (column 2 lines 23 – 45).

**As to claim 5,** Tsai et al disclose (fig 5) a circuit board having a boundary scan self-testing function of Claim 1, wherein the substrate further includes at least one I/O port (fig 5, port at TDO terminal) for outputting test results of the active testing device.

**As to claim 6,** Tsai et al disclose (fig 5) a circuit board having a boundary scan self-testing function of Claim 4, wherein the substrate includes test access ports having a short circuit between the TDI and TDO.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen at (703) 306-5858. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4900.

JN.  
August 18, 2004



**Michael Tokar**  
**Supervisory Patent Examiner**  
**Technology Center 2800**